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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/651,944	08/31/00	DRAPKIN	ATI-000152BT

EXAMINER	
NGUYEN,H	
ART UNIT	PAPER NUMBER
2816	

025310
VOLPE AND KOENIG, PC
DEPT ATI
SUITE 400, ONE PENN CENTER
1617 JOHN F KENNEDY BLVD
PHILADELPHIA PA 19103

MMC2/0328

DATE MAILED: 03/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/651,944	Applicant(s) DRAPKIN ET AL.	
	Examiner Hiep Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the corr spondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☐ Responsive to communication(s) filed on *31 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 5, the recitation "would be" in line 6 is indefinite because it is not a positive recitation.

Claims 6-7 are also indefinite because they depend on the rejected base claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Cave et al. (US Pat. 4,590,389).

Regarding claims 1 and 12, figure 3 of Cave shows a method for reducing distortion of a signal applied to an input of a circuit having a parasitic capacitance, comprising the steps of: detecting a direction of change in voltage of input signal Vin (34); and introducing a current (I) to the parasitic capacitance (C1) to compensate for current of the input signal charging the parasitic capacitance (C1) responsive to detection of a positive edge of said input signal. When the input signal Vin goes high, transistor (34) is turned on and transistor (42, having the collector connected to node 40) charges the parasitic capacitance (C1) with current I.

Regarding claim 2, the signal is applied to an input of an input/output device (30)

Regarding claims 3 and 13, the detection circuit (34) detects direction of change in voltage of the input signal (Vin); and prevents discharge of the parasitic capacitance responsive to detection of a negative edge of the input signal (transistor 34 turns off at the negative edge of Vin).

Regarding claims 4 and 11, transistor (34) detects a change in voltage of the input signal (Vin); and changes an impedance of a parallel termination circuit (2, 38, 22) that is in parallel with the parasitic capacitance (C1) to reduce distortion of the input signal. Note that the positive edge of Vin turns transistors (34, 42) on and the termination circuit (2, 38, 22) is turned on and a current (I) is injected to node (40) thus the impedance of the termination circuit changes.

Regarding claim 5, the detection circuit (34) detects a change in voltage of the input signal (Vin); and a correction circuit (42) coupled to the detection circuit for compensates the current from the input signal that is diverted to the parasitic capacitance due to a positive edge of said input signal.

Regarding claim 6, the capacitance is inherently included inside the transistor (34).

Regarding claim 7, circuit (30) is an input/output device.

Regarding claim 8, a detection circuit (34) detects a change in voltage of the input signal (Vin); and a correction circuit (42) coupled to the detection circuit (34) for preventing current from the parasitic capacitance (C1) to be added to the input signal due to a negative edge of said input signal. Note that at the negative edge of the input signal transistor (34) is turned off.

Regarding claim 9, the capacitance is inherently included inside the transistor (34).

Regarding claim 10, circuit (30) is an input/output device.

Claims 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (US Pat. 6,091,656).

Regarding claim 14, figure 22 of Ooishi shows 14 an apparatus for reducing distortion of a signal applied to an input (OUT) of a circuit operating at high frequency and having a parasitic capacitance, comprising: a first circuit element (162) for selectively providing current to the parasitic capacitance (Cm, included in line 110 and 150) when QP and 162 are turned on; a second circuit element (163) for selectively preventing discharge of the parasitic capacitance (Cm) into the input (OUT, when NQ and 163 are turned off), and a control circuit (G) monitoring input signal for respectively turning on the first circuit element and turning off said second circuit element when a positive going edge of said input signal is detected and for turning off said first circuit element and turning on said second circuit element when a negative going edge of the input signal is detected.

Regarding claim 15, the parasitic capacitance is included between Vc and Vs.

Regarding claims 16 and 17, the first and second circuit elements are (162 and 163).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen

Examiner

03-23-2000

TUAN T. LAM

PRIMARY EXAMINER